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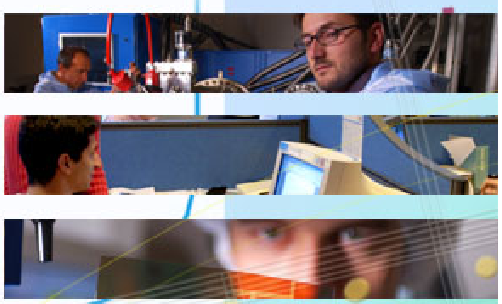
What is 3D IC integration and what metrology is needed?

Patrick Leduc



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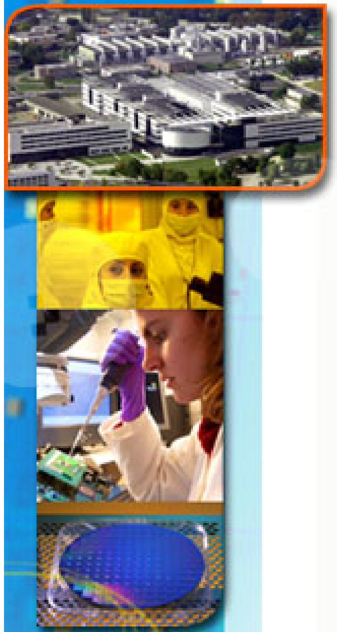


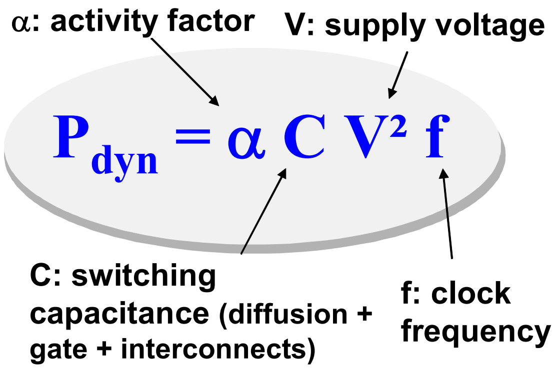
Outline

- Challenges of advanced interconnects
- 3D integration for Integrated Circuits (3D ICs)
- Applications for 3D ICs
- 3D IC technologies: Integration approaches and main players
- Metrology needs for 3D integration
  - Alignment accuracy during wafer bonding
  - Bonding interface quality
  - Substrate thinning quality
  - Via realization (patterning, isolation and filling)
- The future of 3D ICs: Hybrid “Nano/CMOS” 3D ICs
- Summary

Challenges of advanced interconnects

- Today, **More than 50%** of dynamic **power consumption** is due to **interconnects.** This rate is projected to increase.

[Nir Magen et al, Proc. of the 2004 international workshop on System level interconnect prediction, France, pp 7-13, 2004]



$$P_{dyn} = \alpha\, C\, V^2\, f$$

α: activity factor

V: supply voltage

C: switching capacitance (diffusion + gate + interconnects)

f: clock frequency

- **Global Interconnect length** doesn't scale with transistors and local wires. Because of functionality increase, chip size remains relatively constant.

[Havemann et al., IEEE, Vol. 89 (5), May 2001]

- **RC delay is increasing exponentially**. For 65nm node, RC delay in 1mm global wire at minimum pitch is ~100 times higher than NMOSFET intrinsic delay [ITRS07].

[ITRS 2007]

Challenges of advanced interconnects

Interconnect performance requirements :

Power consumption
Communication speed
Signal integrity

Materials, processes :

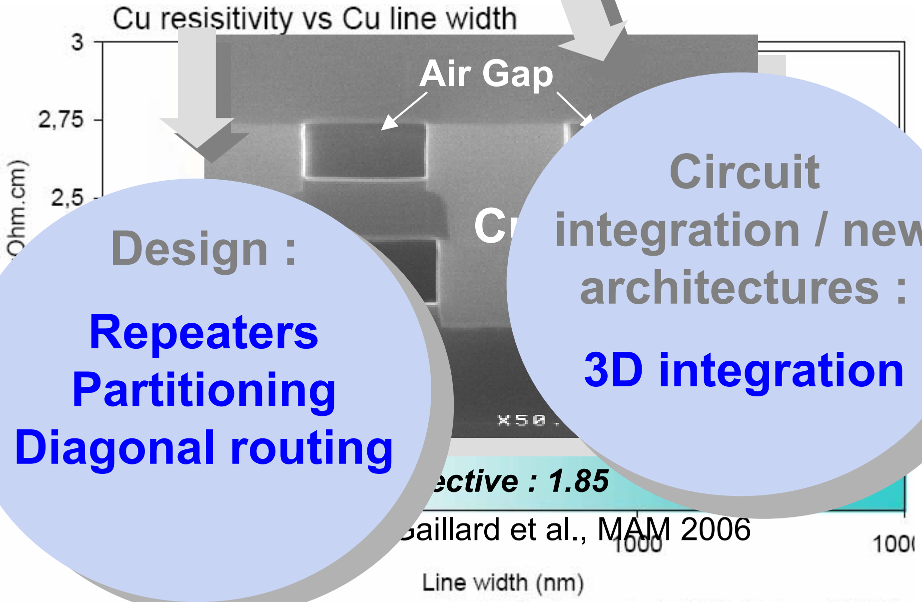
Line resistance (R)
Coupling (L, C)

Design :

Repeaters
Partitioning
Diagonal routing

Circuit integration / new architectures :

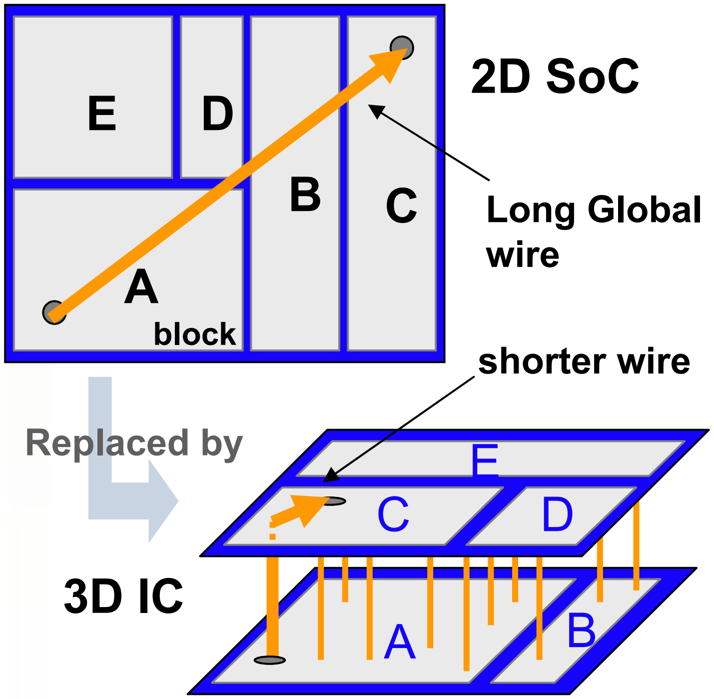
3D integration



S. Maitrejean et al. MRS Spring (2006)
PH Haumesser et al. Fabtech (2006)

3D integration for ICs

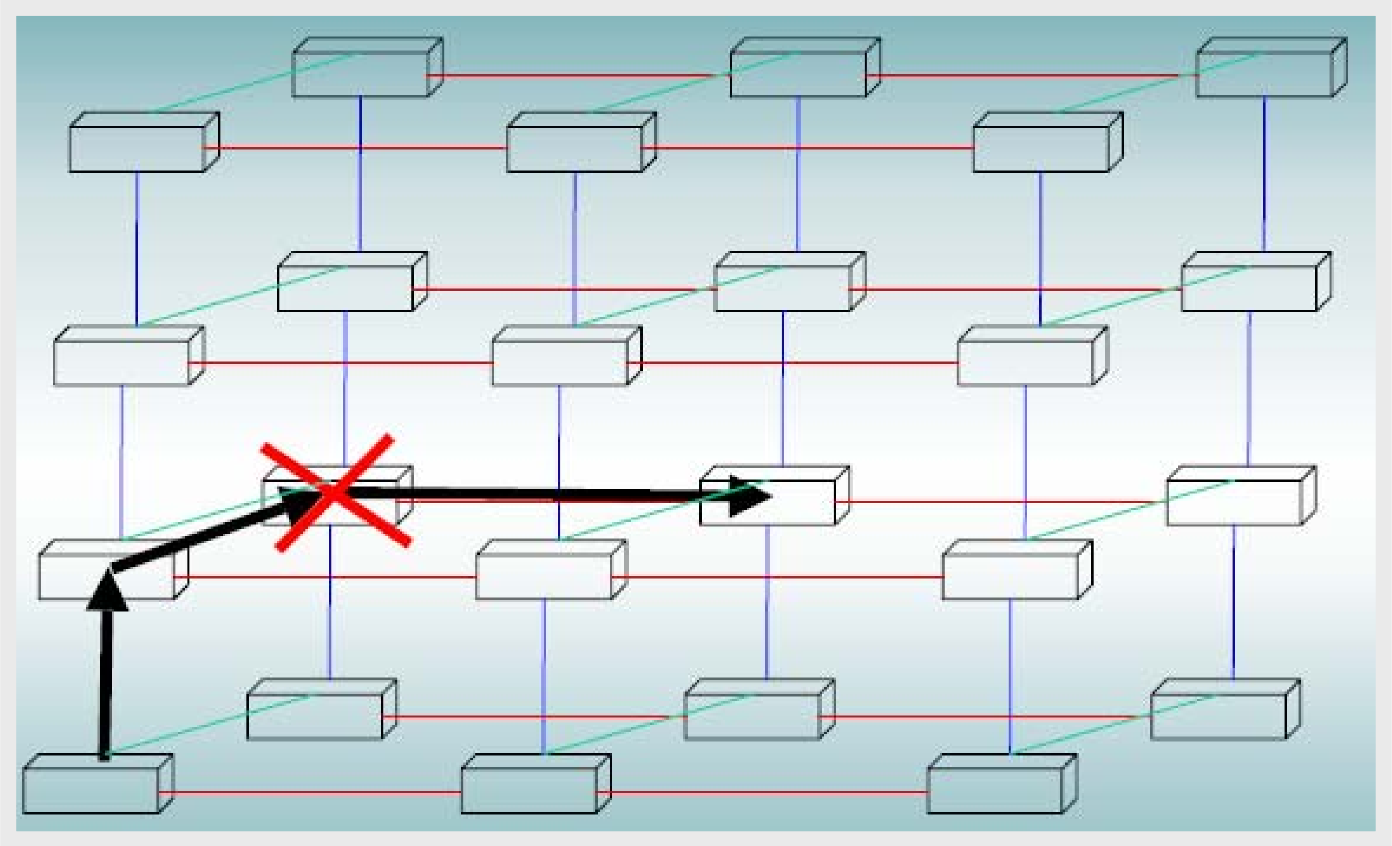
- **3D integration** consists of stacking Integrated Circuits and connecting them vertically



- Replacing long horizontal with short vertical interconnects
  - Addressing **RC delay, crosstalk and power consumption**
  - Reducing **form factor**
- Enabling the integration of heterogeneous devices and technologies (Memory, logic, RF, analog, sensors, …)
  - **Cost reduction** compared to SoC
  - Enable new **functionalities**
- Enable higher fault resistance thanks to the high connectivity of 3D IC.

3D integration for ICs

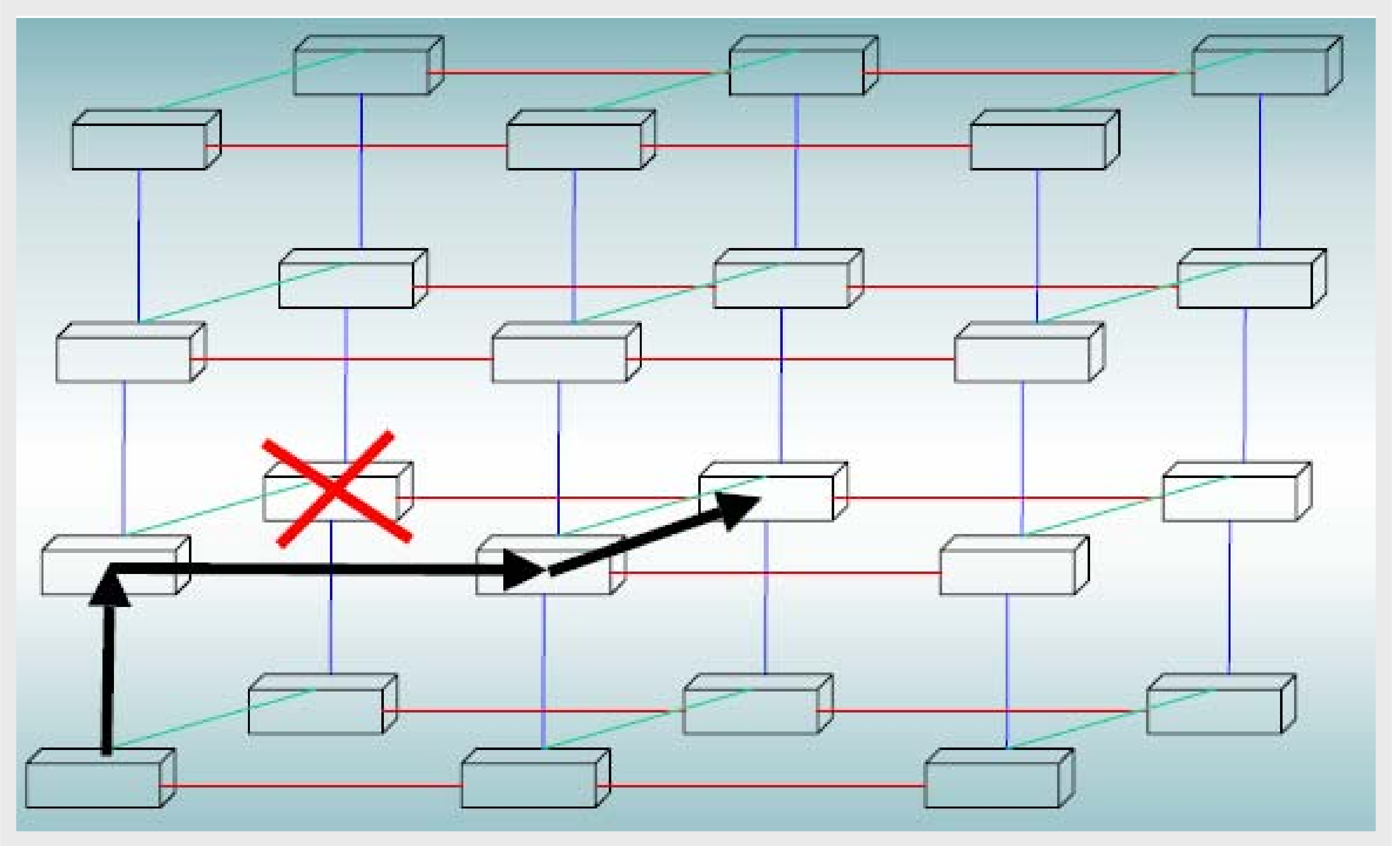
- **Fault resistance**



Bob Patti (Tezzaron), Conference on 3D Architectures for Semiconductor Integration and Packaging, 31oct-2nov 2006, SF, CA

3D integration for ICs

- **Fault resistance**



Bob Patti (Tezzaron), Conference on 3D Architectures for Semiconductor Integration and Packaging, 31oct-2nov 2006, SF, CA

3D integration for ICs

“*Fusion Era*”

- “We are at the doorstep of the **largest shift in the semiconductor industry ever**, one that will dwarf the PC and even the consumer electronics eras”
- “The core element needed to usher in the new age will be a complex integration of different types of devices such as memory, logic, sensor, processor and software, together with new materials, and advanced die stack technologies, … **all based on 3D silicon technology**”

Dr. Chang-Gyu Hwang, president-CEO, Samsung Semiconductor, IEDM conference, Dec. 2006

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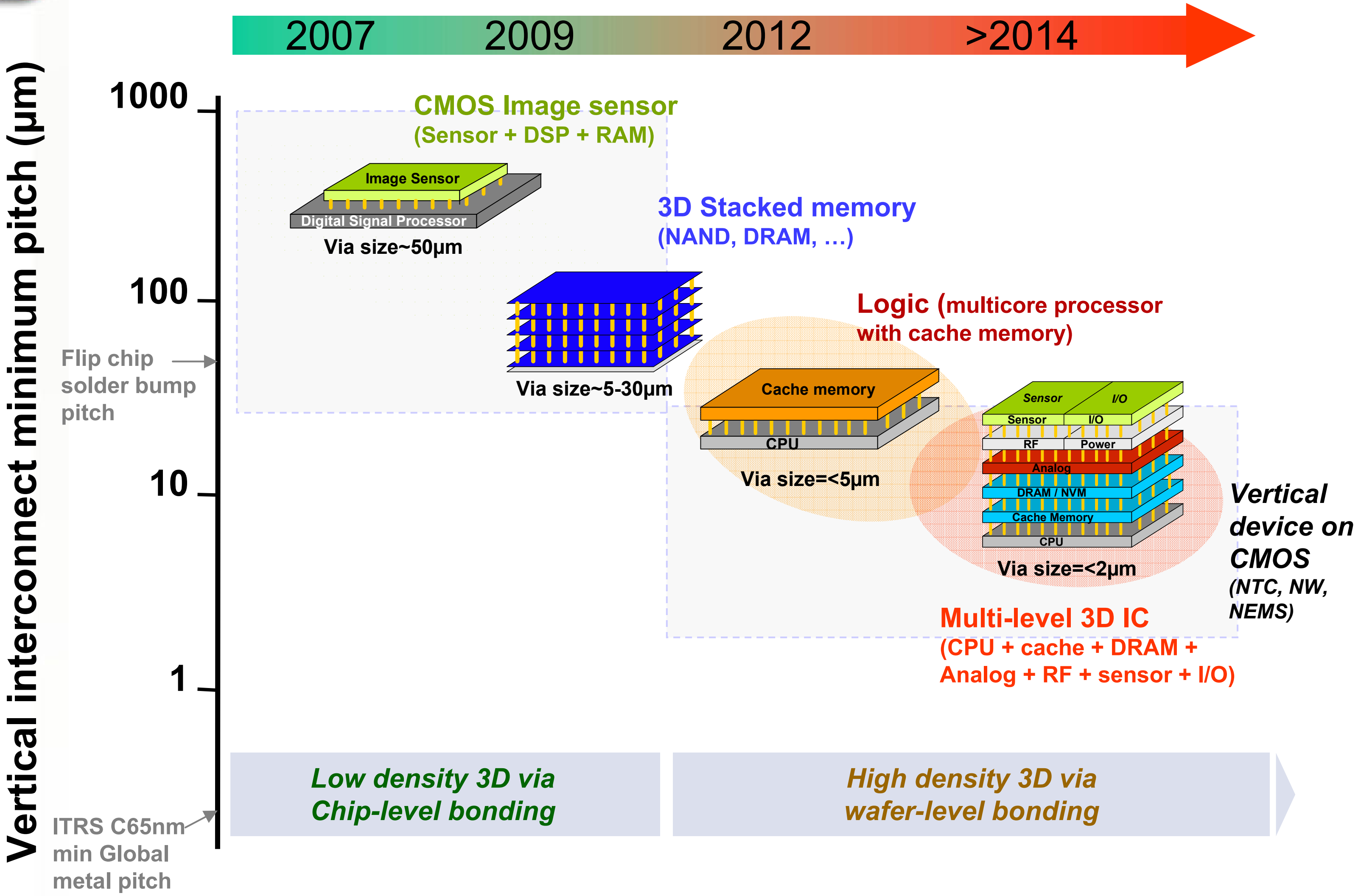
Applications of 3D integration



CMOS Image sensor
(Sensor + DSP + RAM)

Via size~50µm

3D Stacked memory
(NAND, DRAM, …)

Via size~5-30µm

Logic (multicore processor with cache memory)

Via size=<5µm

Via size=<2µm

Multi-level 3D IC
(CPU + cache + DRAM + Analog + RF + sensor + I/O)

Vertical device on CMOS
(NTC, NW, NEMS)

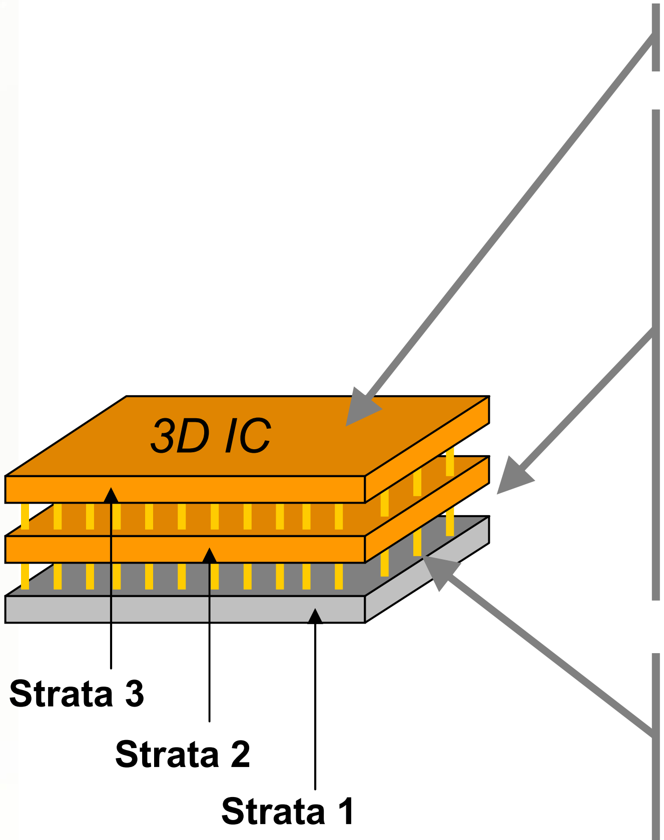
Flip chip solder bump pitch

ITRS C65nm min Global metal pitch

Low density 3D via
Chip-level bonding

High density 3D via
wafer-level bonding

3D IC technologies



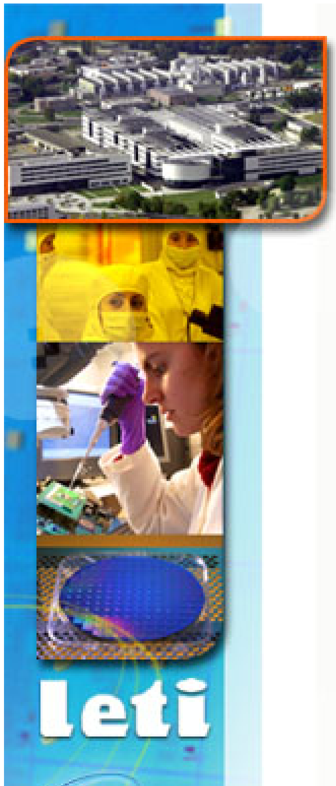
Substrate: SOI or Bulk Si

Bonding technique:

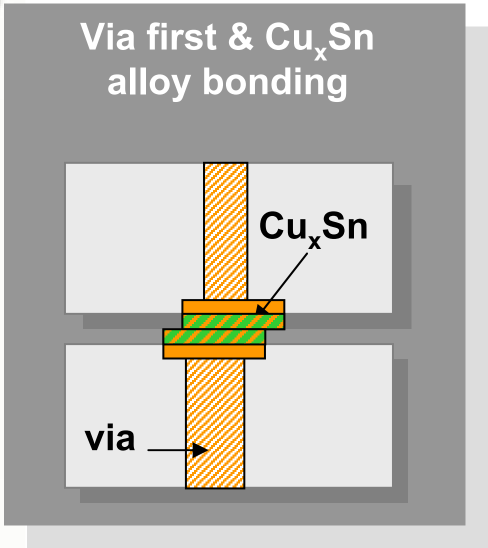
- Die-to-die, die-to-wafer, wafer-to-wafer
- Before or after substrate thinning
- Face-to-face or face-to-back
- Direct bonding (SiO2), bonding with glue, metallic bonding (Cu, SnCu alloy)

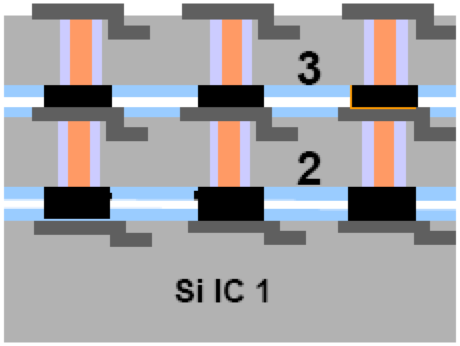
Via realization:

- Via first: pre-process (Front-End), Mid-process (after contact), post-process (after Cu interconnects)
- Via last: after bonding
- Cu, W, poly Si

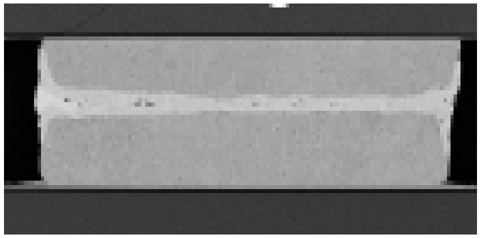


Via first & Cu$_x$Sn bonding (w/ or w/o glue)

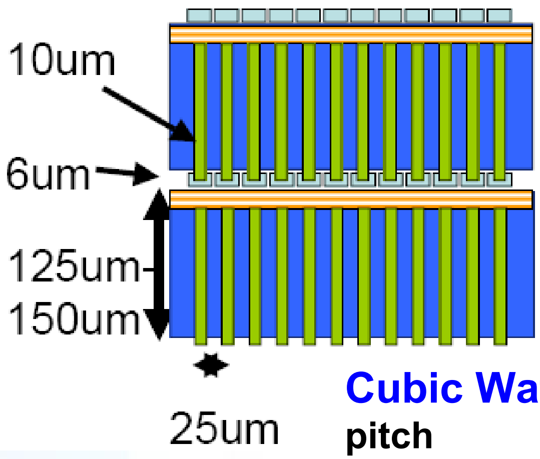


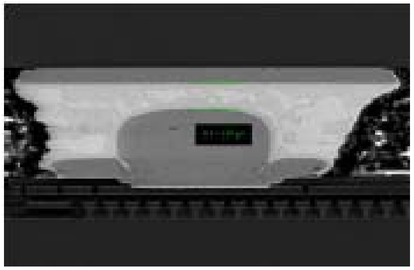


K. Williams et al., 3D Architectures for Semiconductor Integration and Packaging Conf., 31oct-2nov 2006, SF, CA



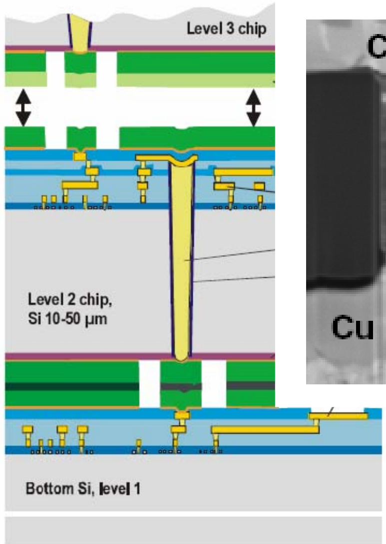
RTI, **Pitch ~20µm, die-to-wafer, glue layer for fine pitch**

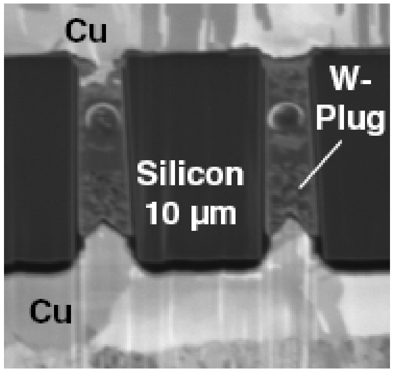




Cubic Wafer, **die-to-wafer, 25µm pitch**

J. Trezza et al., 3D Architectures for Semiconductor Integration and Packaging Conf., 31oct-2nov 2006, SF, CA

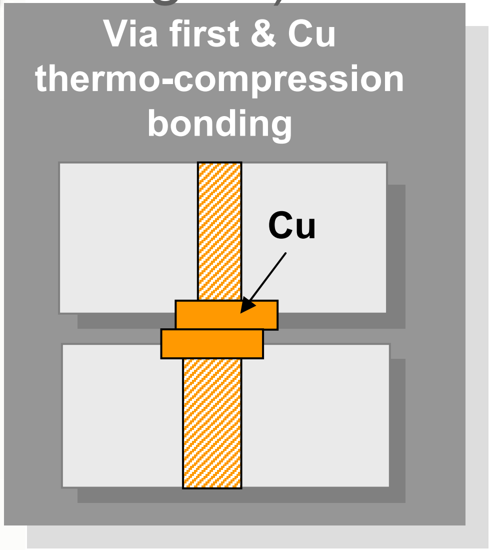




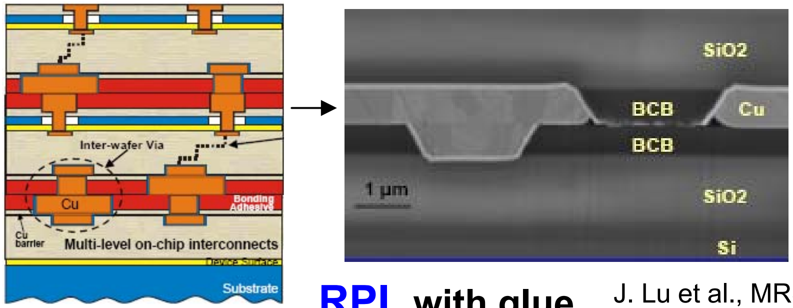
Fraunhoffer IZM, **Pitch <15µm**

B. Wunderle et al, MRS fall 2006

Via first & Cu thermo-compression (w/ or w/o glue)

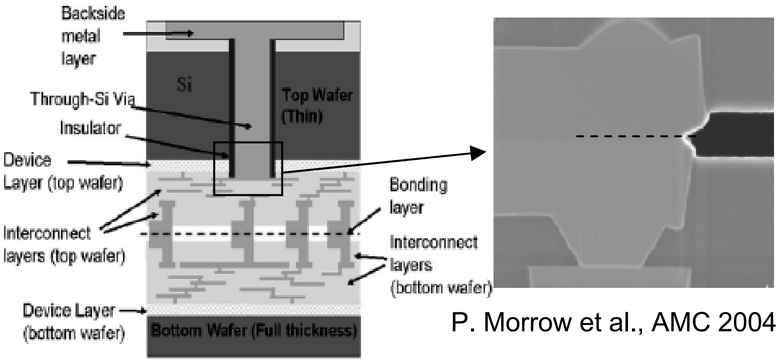


Via first & Cu thermo-compression bonding



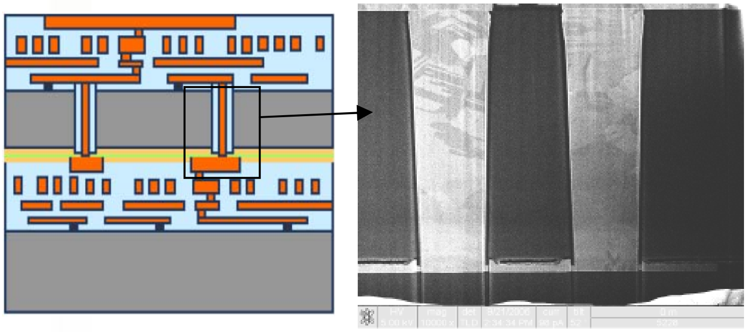
RPI, with glue

J. Lu et al., MRS Spring 2005



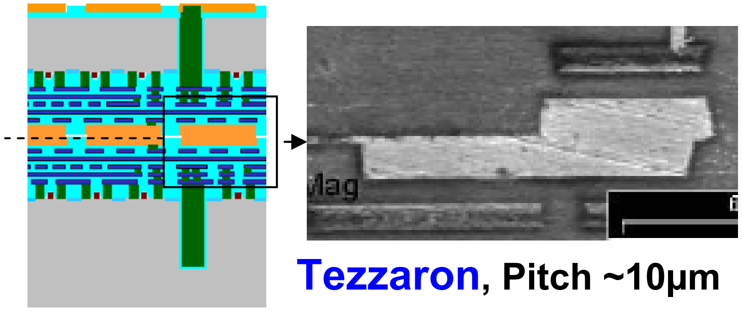
P. Morrow et al., AMC 2004

Intel, Pitch <10µm



IMEC, Pitch ~10µm

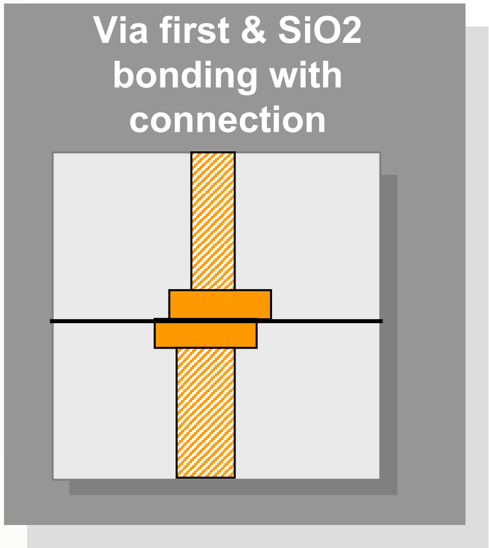
P. De Moor et al., MRS fall 2006

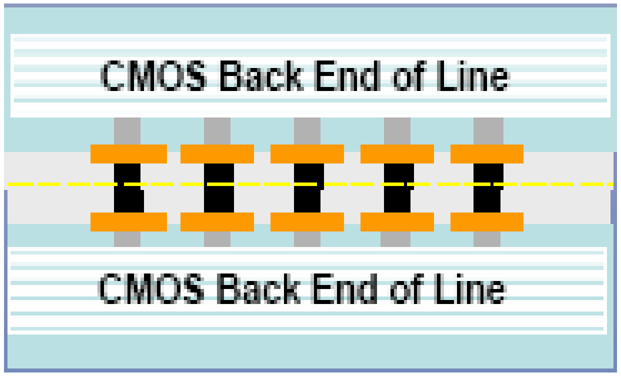


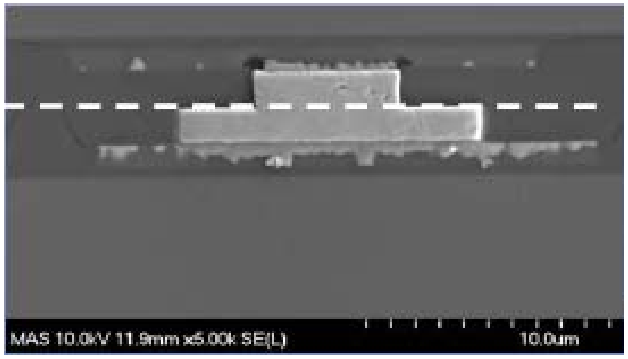
Tezzaron, Pitch ~10µm

R. Patti et al., RTI Conf., 2006,

Via first & SiO$_2$ direct bonding


Via first & SiO2 bonding with connection

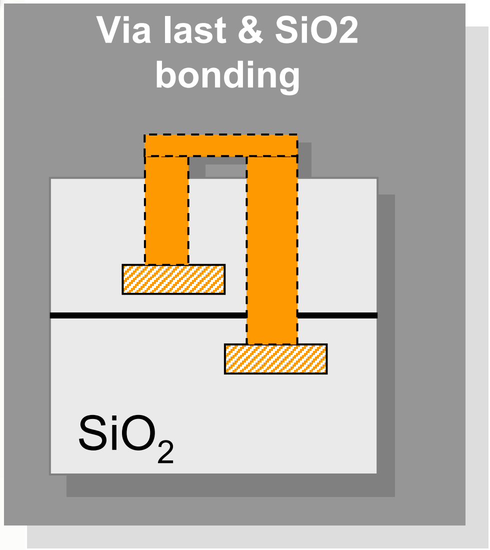


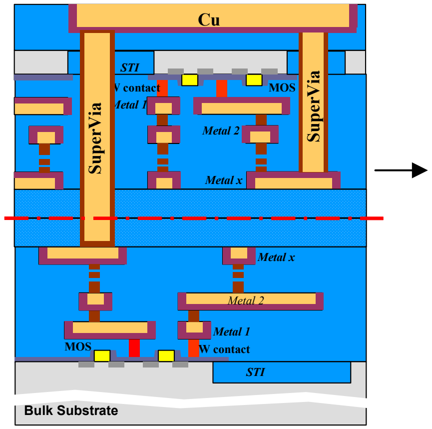


Ziptronix, SiO$_2$ bonding (DBI^{TM}), pitch <10µm

P. Enquist et al., 3D Architectures for Semiconductor Integration and Packaging Conf., 31oct-2nov 2006, SF, CA

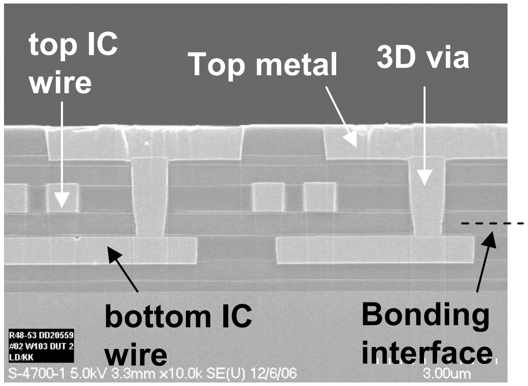
SiO$_2$ bonding & via last


Via last & SiO2 bonding

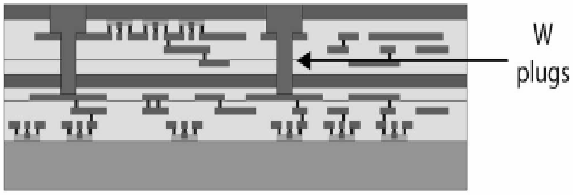


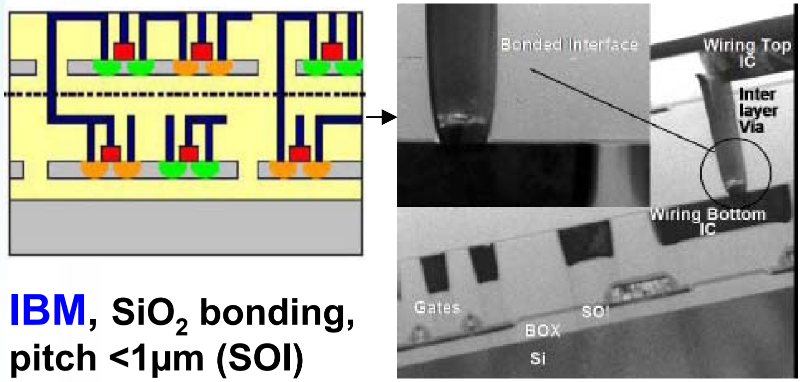
R. Chatterjee et al., IITC 2007 (To be published)

P. Leduc et al. IITC 2007 (To be published)



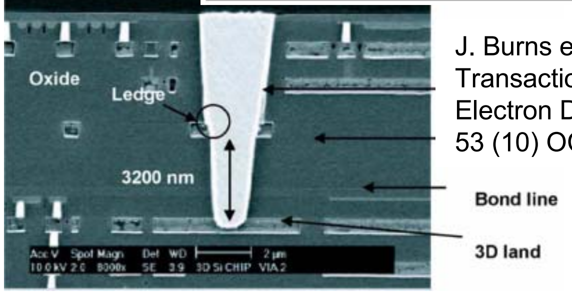
CEA Léti - MINATEC / Alliance, SiO$_2$ bonding, pitch ~5µm (SOI)





IBM, SiO$_2$ bonding, pitch <1µm (SOI)

A.W. Topol et al., IEDM 2006

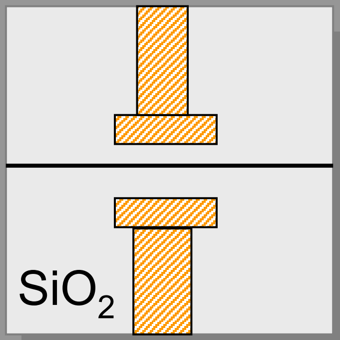


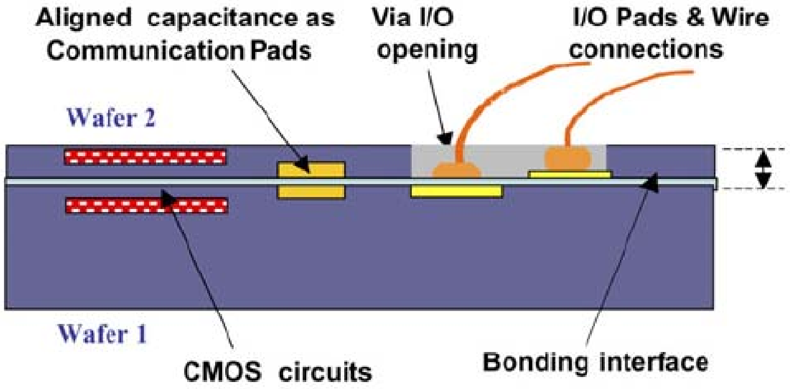
J. Burns et al., IEEE Transactions on Electron Devices, Vol. 53 (10) OCt. 2006

MIT Lincoln (SOI), 8µm pitch

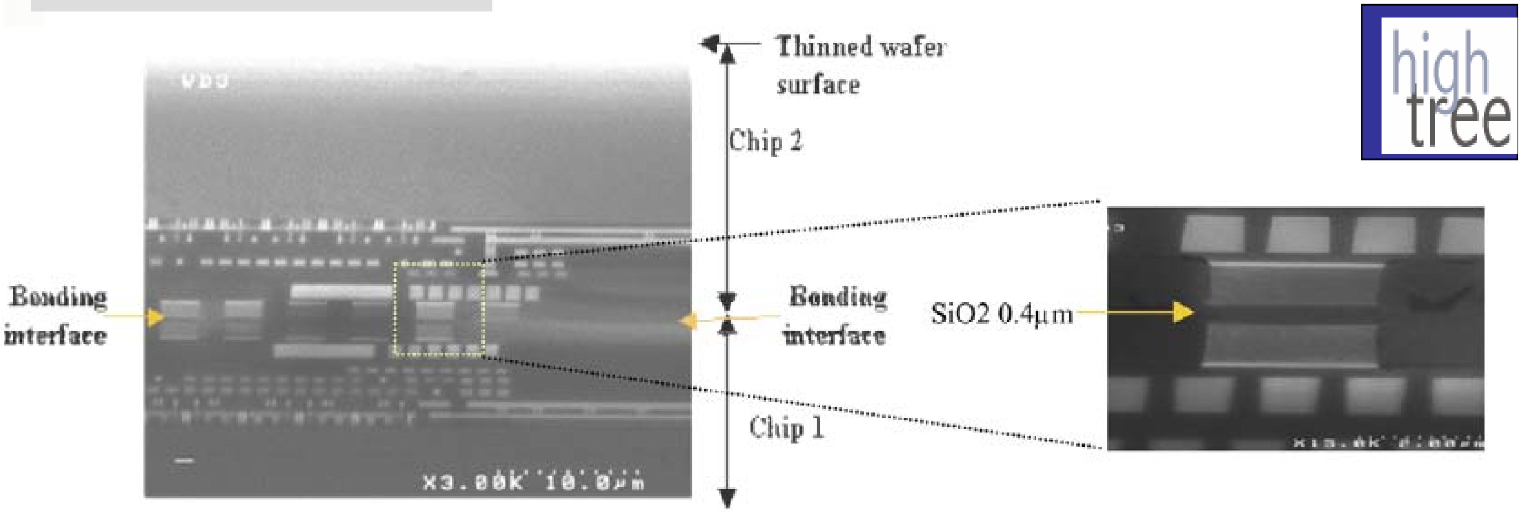
SiO$_2$ bonding & Capacitance coupling

Capacitance interconnect (SiO2 bonding)

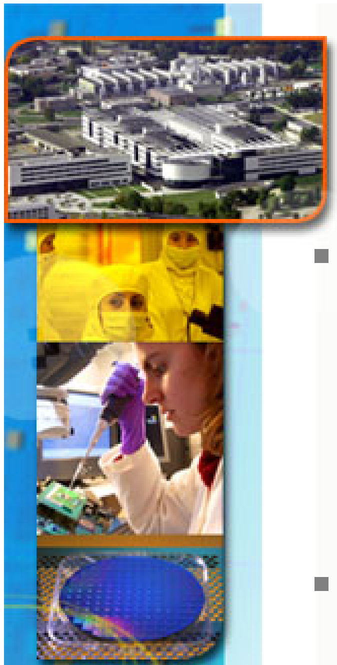




CEA Léti - MINATEC / ST / Univ. of Bologna



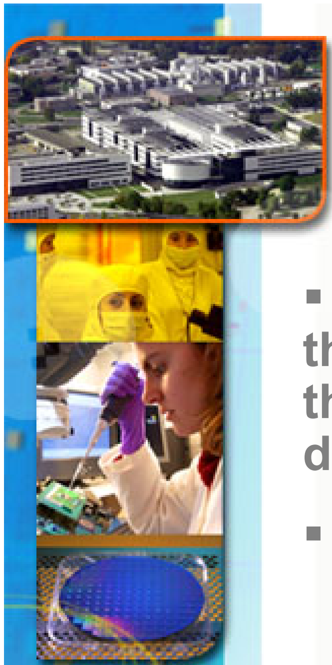
B. Charlet et al., MAM 2006



2007

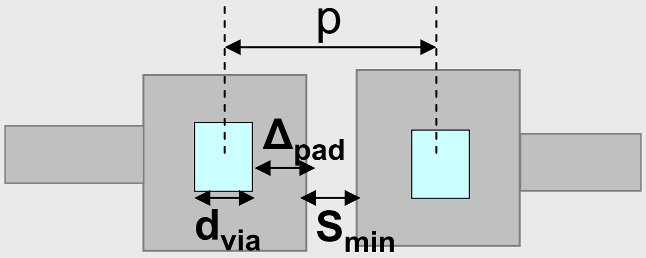
3D IC technologies

- Generic technologies to be developed
  - **Bonding with alignment** (face-to-face and face-to-back)
  - **Si thinning** (Si bulk and SOI substrates)
  - **3D via realization**
- Design/Reliability concerns
  - **Thermal management** => specific heat spreader needed?
  - **Electrical coupling** => specific design rules needed?
- Associated metrology and characterization
  - **Wafer alignment accuracy** (during bonding)
  - **Bonding quality** (interface defects, adhesion strength)
  - **Si thinning** (thickness control, roughness, surface defects, crystalline defects, stress relaxation, wafer edge control for post-processing)
  - **Via realization** (filling quality, electrical contact, reliability)



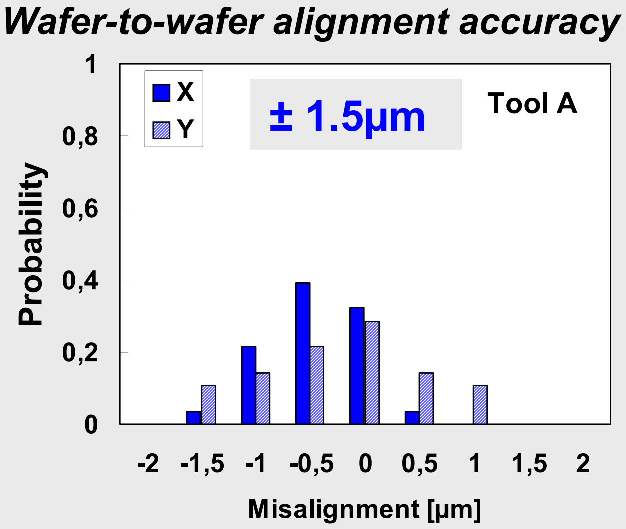
Alignment accuracy during bonding

- **Alignment accuracy** determines the pad size and, by consequence, the maximum vertical interconnect density.
- It depends on bonding technique:
  - Face-to-Face ⇔ Face-to-Back
  - Glue ⇔ Direct bonding
  - Die-to-Wafer ⇔ Wafer-to-Wafer
- It depends also on:
  - Wafer flatness
  - Wafer co-planarity
  - Heat uniformity and mechanical noise during alignment and bonding.

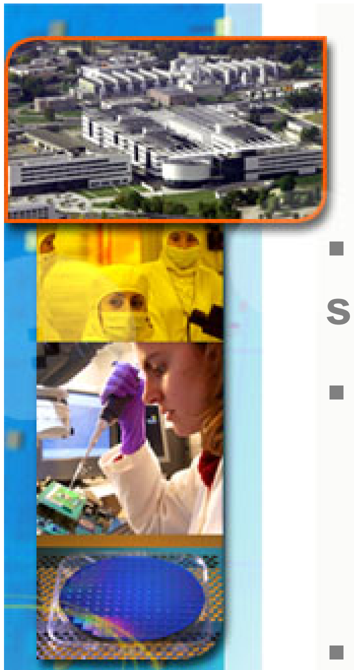


$$P = \Delta_{pad} + d_{via} + S_{min}$$

R. Chatterjee et al., to be published at IITC 2007



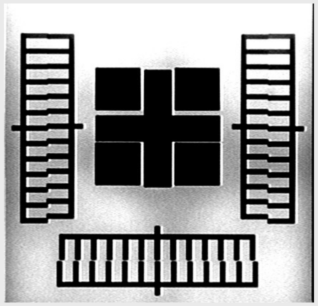
P. Leduc et al., to be published at IITC 2007



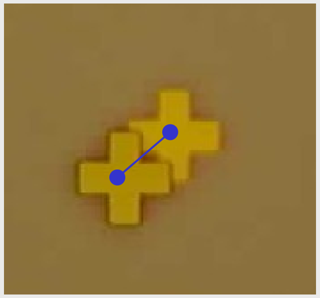
Wafer-to-wafer alignment

- **Non-destructive alignment control** is challenging because of silicon substrate non-transparency in visible light (λ < 1µm)
- Alignment control after bonding and **before substrate thinning**:
  - **IR microscopy** needed trough thinned bulk silicon
  - Relative **low resolution** (λ ~1µm)
- Alignment control after bonding and **after substrate thinning**:
  - **Advantage of SOI substrate** (no bulk Si left after thinning)

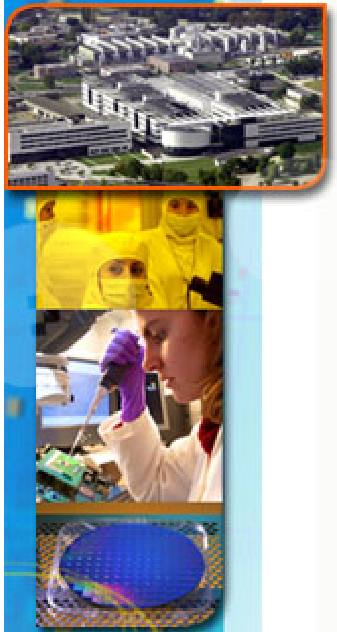
IR image
(bulk Si)



Visible image
(SOI after thinning)



CEA Léti - MINATEC



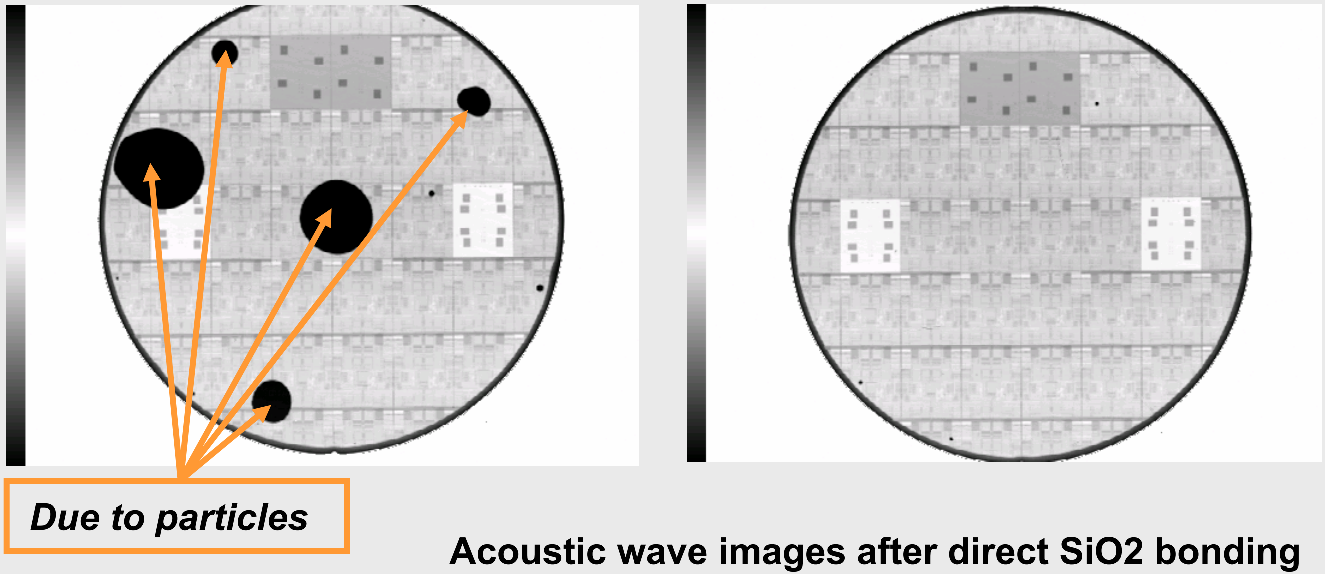
Wafer bonding quality

- **Process requirements**:
  - Low temperature process, compatible with BEOL (T<400°C))
  - Low interface defectivity and high interface adhesion

- **Characterization and metrology**:
  - Before bonding:
    - Initial wafer curvature (maximum wafer bow and wrap)
    - Surface roughness, flatness, hydrophobic properties for dielectric bonding, contamination
  - After bonding:
    - Interface defectivity
    - Interface adhesion

Wafer bonding quality

- **Interface defectivity** => non-destructive metrology needed
  - Interface control through non-transparent Si bulk
  - IR and Acoustic Microscopy: low resolution (<λ)
  - Interface control with circuits



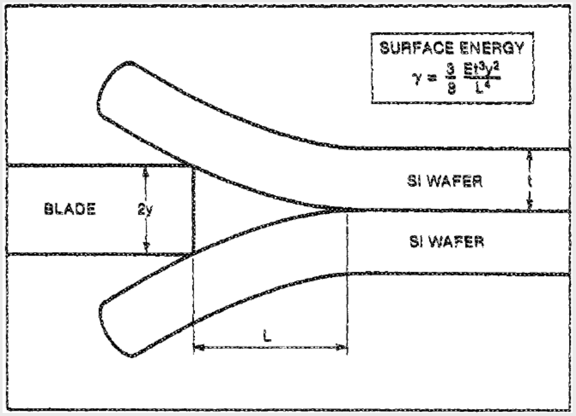
Acoustic wave images after direct SiO2 bonding

CEA Léti - MINATEC

Wafer bonding quality

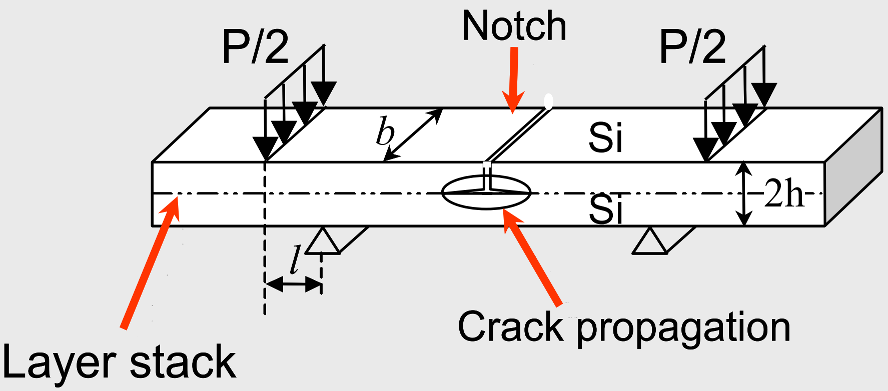
- **Interface adhesion measurement**:
  - Wedge-opening test (Maszara technique) need to be adapted to patterned wafers (with interconnects)
  - 4-pts bending technique can be used (the correlation with Maszara technique is not obvious: different phase angle)

W.P. Maszara et al., J. Appl. Phys., 64 (10), Nov 1988

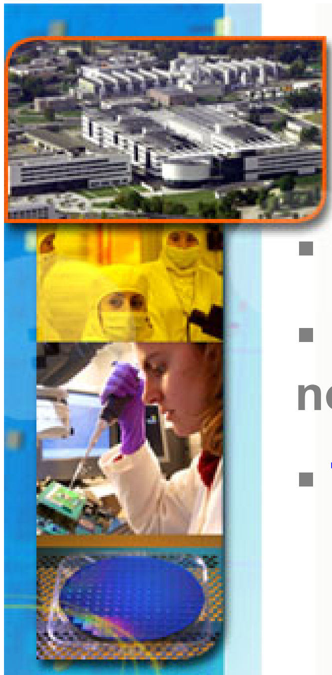


Wedge-opening test

R.H. Dauskardt et al., Eng. Fract. Mech. 61 (1998)141-162

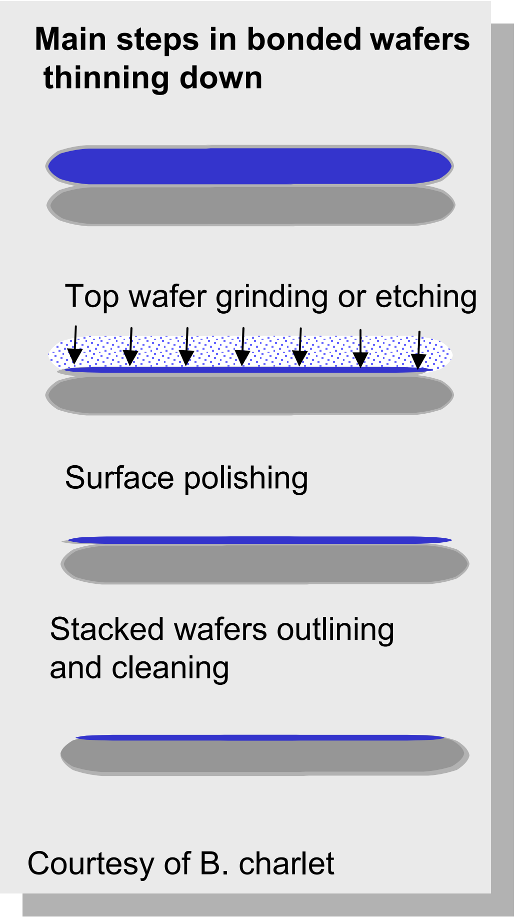


4-pts bending test



Substrate thinning

- **SOI substrate**: etch stop layer
- **Si bulk substrate** (thinned down to <10µm): no etch stop layer…
- **Thickness control**:
  - In-situ metrology needed for Si thickness uniformity control and endpoint detection (FTIR spectroscopy, …)
  - With circuits: effect of dopants, devices, etc… on thickness control (micro-focusing needed)
- **Compatibility with FEOL devices**:
  - Stress relaxation in Si (Raman Spectro.)
  - Crystalline defects in Si (chemical decoration, X-ray topography, TEM)
  - Surface contamination control (metallic contamination, particles)



Main steps in bonded wafers thinning down

Top wafer grinding or etching

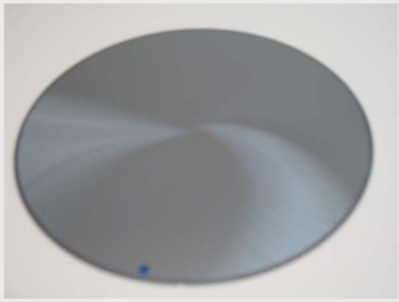
Surface polishing

Stacked wafers outlining and cleaning

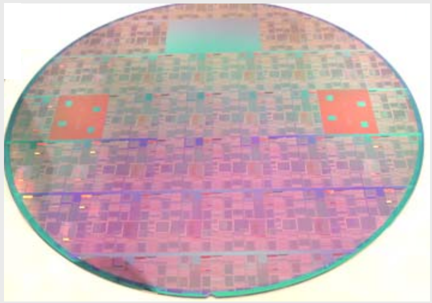
Courtesy of B. charlet

Substrate thinning

- **Compatibility with BEOL interconnects**: Interconnect (ULK/air-gap) mechanical integrity
- **Compatibility with 3D integration**: Bonding interface integrity if the Si thinning if performed after bonding (especially with multi-layer stacking)
- **Compatibility for post-thinning process**:
  - Wafer edge quality
  - Surface quality (roughness, contamination)

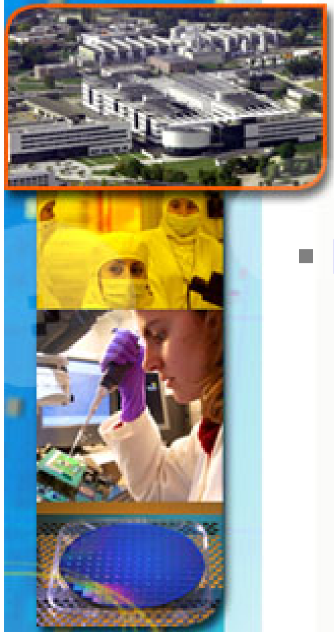


Thinned Si Bulk (10µm)



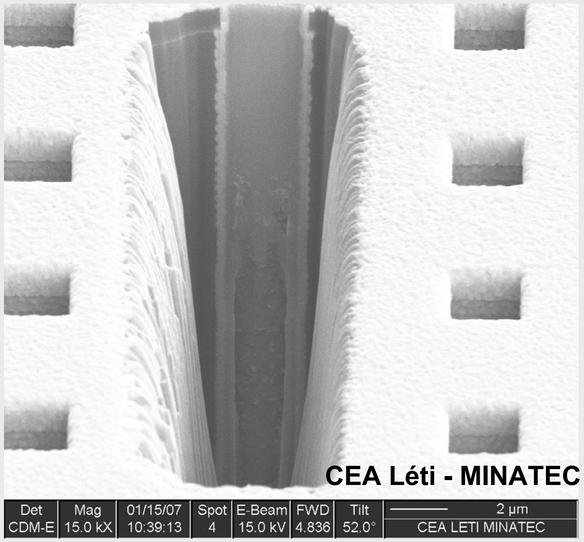
Thinned SOI

CEA Léti - MINATEC

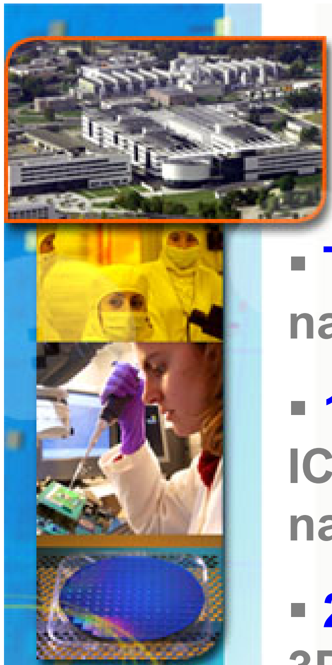


3D Super-Via realization

- **Process requirement**:
  - BEOL thermal compatibility (T<400°C)
  - FEOL electrical compatibility: minimal capacitance coupling, metallic contamination in silicon
  - High aspect ratio (AR) => void management
- **Metrology**:
  - Etching – filling: FIB-SEM / TEM observation => deep via !!
- **Electrical characterization and Reliability**:
  - Via/Pad contact resistance
  - Thermo-mechanical stress



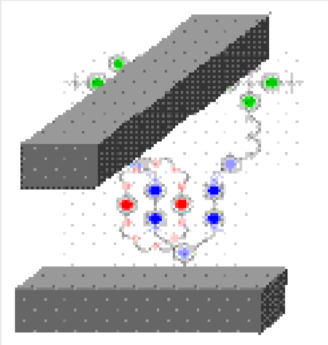
FIB-SEM image of 3µm-wide / 15µm-deep super-via after copper seed layer deposition



Future of 3D ICs: Hybrid 3D ICs

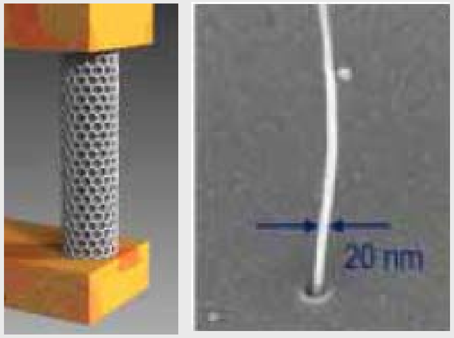
- **The future of 3D ICs** consists of co-integrating nanomaterials to CMOS.
- **1st objective**: use 3D technology to increase IC functionality and performance thanks to nanomaterials properties.
- **2nd objective**: adapt actual technology to real 3D technologies with vertical devices.
- **Characterization and metrology challenges** : characterization of single nanomaterial, and characterization of nanomaterial properties in their environment.

CMOL (CMOS / Molecular)

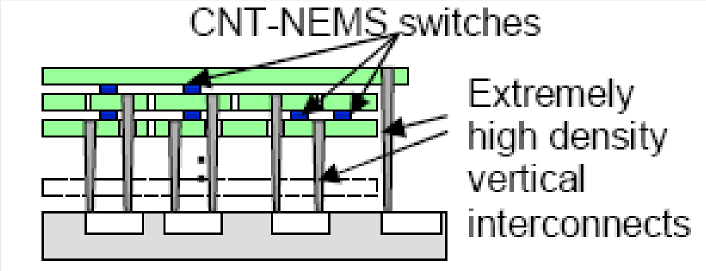


Stan et al., VLSI Design 2006

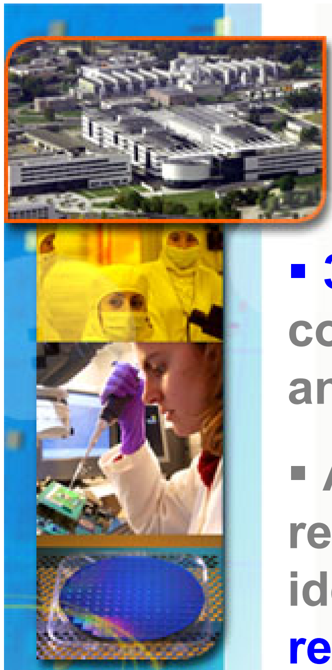
Carbon Nanotube



Franz Kreupl, Microelectronic Engineering, Vol. 64, (1-4) Oct. 2002, Pp. 399-408

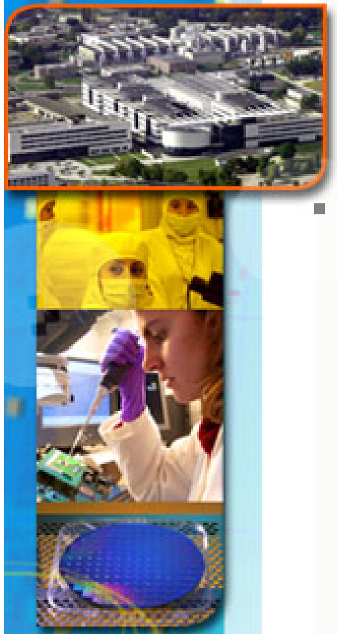


S. Fujita et al., Conference on Nanotechnology, IEEE, Vol. 1, Pp. 314-317, June 2006



Summary

- **3D integration** enables improvements in IC performance, power consumption, system functionality and form factor. 3D technology is an alternative solution to scaling issue in CMOS circuits.
- A lot of specific 3D technologies are being developed in parallel in research centers. Nevertheless, several **generic technologies** can be identified as **bonding with alignment**, **Si thinning** and **3D via realization.**
- Several **metrology and characterization challenges appear:**
    - **Wafer alignment accuracy** during bonding
    - **Bonding interface defectivity and adhesion control through silicon**
    - **In-situ Si substrate thickness control during Si thinning (with circuits)**, CMOS compatibility (stress, crystalline defects, ULK/Air-Gap integrity)
    - **Via realization** (filling quality, electrical contact, reliability)
- **For future Hybrid 3D ICs, characterization and metrology challenges** will be linked to the characterization of single nanomaterial properties in their environment.



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